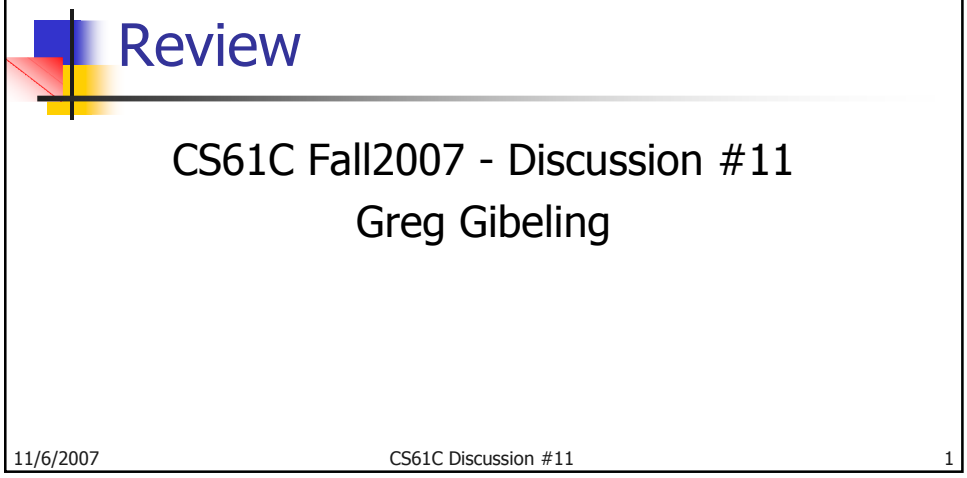
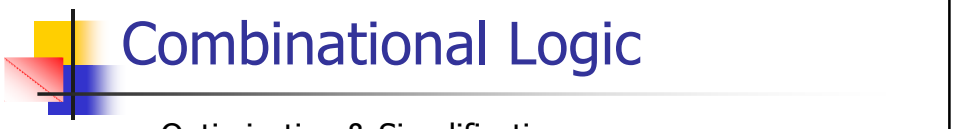


CS61C: Hardware & CPU Review

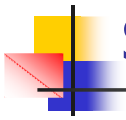
CS61C Fall2007 - Discussion #11

Greg Gibeling



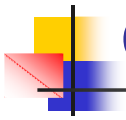
Combinational Logic

- Optimization & Simplification
  - Constant Propagation
  - Common Subexpressions
  - Truth Tables
  - Don't Care Inputs & Outputs (Not the same!)
- Special Gates
  - OR: Detect 0
  - AND: Detect 1
  - XOR: Compare, Conditional Invert, Add
  - Mux, NAND: Universal
- Delay & Cost
  - Critical Path (Quiz)
  - Gate Count (Proj4 in simple gates!)



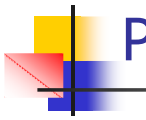
State

- Registers
  - Delay of one clock cycle
  - Storage (assuming Enable control)
  - Connection through time
- Datapath
  - Generally registers are data storage
  - Pipeline registers?
- FSMs
  - Bubble & Arc Diagrams
  - State & Output Encoding
  - Single register, two CL blocks



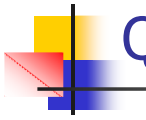
General SDS Design

- Datapth
  - Value Registers
  - Mostly Combinational Logic
    - Almost all of it ~32b (or some fixed #) wide
  - Mux & Control Inputs
- Control
  - Decode – Sum of Products
  - Stateful Control (Multi-cycle Designs)
- How To
  - Draw the schematic
  - Work out the timing diagrams
  - Code in Verilog
  - Test



Pipelining

- Basic Tradeoff
  - Throughput: increased
  - Latency: unaffected (slight increase, why?)
- Design
  - Add registers in the middle of the proc
  - Forwarding logic
- Dependencies
  - Control (Branches)
  - Data
    - RAW – True Data Dependence
    - WAW – Not a problem?
    - WAR – Not a problem?



Questions/Examples

- Questions
  - Proj4 Clarifications
  - Why x86?
  - Variable Latency Instructions
- Problems
  - Memory-To-Memory Processor
  - Implement MicroCode
  - Design Out of Order Processor (OOO/Tomasulo)